	Application No. Applicant(s)		
Notice of Allowability	09/765,478	BHASIN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	•
The MAILING DATE of this communication apperation apperation allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	ears on the cover sheet w (OR REMAINS) CLOSED in or other appropriate common GHTS. This application is	ith the correspondence address n this application. If not included unication will be mailed in due course	
1. This communication is responsive to 7/20/04.			
2. The allowed claim(s) is/are <u>1-20</u> .		•	
3. $\boxtimes$ The drawings filed on <u>18 January 2001</u> are accepted by the	e Examiner.		
4.			
Attachment(s)  1. Notice of References Cited (PTO-892)  2. Notice of Draftperson's Patent Drawing Review (PTO-948)  3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date  4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ☐ Interview S Paper No. 8), 7. ☐ Examiner's 8. ☑ Examiner's 9. ☐ Other	oformal Patent Application (PTO-152)  summary (PTO-413),  /Mail Date Amendment/Comment  Statement of Reasons for Allowance	•

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## **REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a sequence based verification technique for verifying the functionality of hardware components that move data between nodes in a computer system. The claimed invention recites (claim 14 as representative of the other independent claims 1 and 8) features such as "...a drive module which starts multiple drive loops that pick up packets from the drive buffer and force the device under test to drive the packets in accordance with the determined sequence, the drive module ensuring that each drive loop satisfies specified timing and relation criteria prior to allowing the drive loop to force the device under test; and

an expect module which starts multiple expect loops that pick up packets driven by the device under test, the expect module ensuring that each expect loop satisfies specified timing and relation criteria prior to allowing the expect loop to expect and pick up a packet driven by the device under test, the expect module raising an error flag if the expected packet does not arrive within a specified time period."

The prior arts of record (Allingham U.S. Patent No. 5,937,182 is an example of such prior arts) teach a design verification system for simulating designs and evaluating the simulation results against a set of expected events. A set of expected events are generated and loaded into an expect buffer. As the simulation proceeds, each modeled device collects data on each event into an event record. Each event record is compared against the set of expected events. If the set of expected events contains an

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entry that matches the event record, the matching entry is removed from the expect buffer. If a matching entry is not found then the event record is flagged as an error.

The prior arts however, do not teach a process loop that (i) is configured to expect a data packet within a specified time period and (ii) picks up the expected packet if the expect packet arrives within the specified time period. As such, modification of the prior art of record can only be motivated by hindsight reasoning. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the limitations set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the claimed inventions. Hence, claims 1-20 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

છ્ય Cynthia Britt Examiner Art Unit 2133

Gruy of Lamarre Primary Examiner